Atty. Docket No. OPP031052US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:	:
Young-Hun SEO	: GROUP ART UNIT: 2818
APPLICATION NO: 10/728,699	:
FILED: DECEMBER 5, 2003	: EXAMINER: VU, DAVID

FOR: TRENCH IN SEMICONDUCTOR DEVICE AND FORMATION METHOD THEREOF

I hereby certify that this document is being facsimile transmitted to the USPTO or deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on _____.

By: _____
~~Jennie Heaton~~ Leanne Konze

DECLARATION UNDER 37 C.F.R. 1.132

Mail Stop AF
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

SIR:

Now comes Young-Hun SEO, who declares and states that:

1. I am the sole inventor of the subject matter disclosed and claimed in the above-identified application. My qualifications are attached hereto as Exhibit A.

2. I have read the above-identified application. I have reviewed U.S. Patent No. 5,910,018 to Jang (hereinafter, "Jang").

3. I understand that the broadest claim of the above-identified application is directed to a method of forming a trench in a semiconductor device, comprising:

forming a sacrificial layer on a silicon wafer and selectively etching the sacrificial layer to form a LOCOS opening having a predetermined width;

performing thermal oxidation on a portion of the silicon wafer exposed through the LOCOS opening to form a LOCOS oxide layer;

etching the LOCOS oxide layer and the silicon wafer to a desired depth to form a trench, the etching being performed such that the LOCOS oxide layer is left remaining on the silicon wafer at an area corresponding to edges of the trench;

removing the remaining region of the LOCOS oxide layer and forming a liner oxide layer in the trench; and

forming an insulation layer such that the trench is filled with a material of the insulation layer.

4. Jang discloses a trench edge rounding method and structure for trench isolation. In the process disclosed by Jang, a LOCOS oxide layer is etched such that no LOCOS oxide layer is left remaining on the silicon wafer.

5. For example, Jang shows a thick oxide layer 28 in FIG. 4, and discloses that "thick oxide layer 28 is grown using a thermal oxidation process" (col. 3, lines 17-19). Jang also explains that, in the process disclosed therein, "the length of lateral oxide extrusion (bird's beak) is short and has little effect on the effective diffusion (active) width" (col. 3, lines 23-25).

6. The disclosure(s) recited in paragraph 5 above clearly indicate to one skilled in the art of semiconductor processing and/or fabrication that thick oxide layer 28 is a LOCOS oxide layer.

7. Jang then states that "(t)he grown oxide layer 28 is then removed leaving a rounded isolation edge as shown in FIG. 5." FIG. 5 shows complete removal of LOCOS oxide layer 28.

8. Jang shows in FIG. 7 an oxide layer 29, "formed thermally on the sides and bottom of trench 8 to anneal any trench etch damage and to encapsulate any defects that may occur." (Col. 4, lines 42-44.) In FIG. 7 of Jang, oxide layer 29 is clearly shown along an

interface with silicon substrate 10, including in the locations where LOCOS oxide layer 28 was removed.

9. The disclosure(s) recited in paragraph 8 above further indicate to one skilled in the art of semiconductor processing and/or fabrication that LOCOS oxide layer 28 is completely removed in the process of Jang.

Further, Declarant sayeth not.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon or therefrom.

SEO, Young-Hun
Young-Hun SEO

August 30, 2005.
Date

EXHIBIT A

Work Experience: Director at DongbuAnam Semiconductor, Inc. since 1998; at present, responsible for Etch process & equipment technology; also worked in Logic Process integration for two years.

Education: Received a B.S. degree, an M.S. degree, and a Ph.D. in Chemical Engineering from Chonbuk National University in 1991, 1993, and 1998, respectively. Studied semiconductor manufacturing processes, that is, plasma etching (ECR, RF) and wet etching (electric etching, UV light etching), CVD, MOCVD, etc., during the M.S. and Ph.D. courses.